



INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Attorney Docket Number	1011-54375-01
Application Number	09/620,021
Filing Date	July 20, 2000
First Named Inventor	Rajski
Art Unit	2133
Examiner Name	Phung M. Chung

U.S. PATENT DOCUMENTS

Copies of U.S. Patent documents do not need to be provided, unless requested by the Patent and Trademark Office. For patents, provide the patent number and the issue date. For published U.S. applications, provide the publication number and the publication date. For unpublished pending patent applications, provide the application number and the filing date.

Examiner's Initials*	Cite No. (optional)	Number	Publication Date	Name of Applicant or Patentee
pme		4,536,881	8.20.1985	Kasuya
		5,870,476	2.9.1999	Fischer
		5,872,793	2.16.1999	Attaway et al.
		5,883,906	3.16.1999	Turnquist et al.
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Examiner's Initials*	Cite No. (optional)	Country	Number	Publication Date	Name of Applicant or Patentee
pme		Europe	EP 0372226	6.13.1990	Bardell
pme		Europe	EP 0438322	7.24.1991	Murase
pme		Europe	EP 0481097	4.22.1992	Diebold et al.
pme		Japan	JP 4-236378	8.25.1992	Diebold et al.
pme		Japan	JP 9-130378	5.16.1997	Fischer English abstract
pme		Europe	EP 0887930	12.30.1998	Tarrab et al.
pme		Japan	JP 11-153655	6.8.1999	Park English abstract

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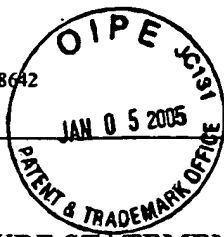
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Examiner's Initials*	Cite No. (optional)	OTHER DOCUMENTS
gme		Bassett et al., "Low-Cost Testing of High-Density Logic Components," <i>IEEE Design & Test of Computers</i> , pp. 15-28 (April 1990).
gme		Fagot et al., "On Calculating Efficient LFSR Seeds for Built-In Self Test," <i>IEEE</i> , pp. 7-14 (1999).
gme		Hellebrand et al., "Generation of Vector Patterns Through Reseeding of Multiple-Polynomial Linear Feedback Shift Registers," <i>IEEE International Test Conference</i> , pp. 120-129 (1992).
gme		Wang, "BIST Using Pseudorandom Test Vectors and Signature Analysis," <i>IEEE Custom Integrated Circuits Conference</i> , pp. 1611-1618 (1998).

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